IN THE CLAIMS

1 (Currently Amended). A method of developing a response compactor comprising:

adding at least two columns to a compactor matrix for each scan chain ~~circuit output~~ that, at the same time as another scan chain, ~~produce~~ produces an unknown logic value.

Claim 2 (Canceled).

3 (Currently Amended). The method of claim 1 [[2]] including obtaining the maximum number of scan chains that can produce unknown logic values at the same time.

Claim 4 (Canceled).

5 (Currently Amended). The method of claim 1 [[2]] including reducing the compactor matrix using maximum compatibility class problem.

6 (Original). The method of claim 5 including eliminating from the matrix one of at least two matching columns.

7 (Currently Amended). The method of claim 1 wherein adding at least two columns to [[a]] the compactor matrix includes adding at least two columns to the compactor matrix for every combination of the number of unknown logic values plus one.

8 (Original). The method of claim 7 including adding values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has the column value zero followed by the column value one and a third row has the column values zero, zero, followed by the column value one.

9 (Currently Amended). A response compactor formed by a process including the steps of:

obtaining a number of circuit outputs from scan chains that can produce unknown logic values at the same time; and

adding at least two columns to a compactor matrix for each such circuit output that, at the same time as another scan chain, produces ~~produce~~ unknown logic values.

10 (Currently Amended). The compactor of claim 9 formed by [[a]] the process wherein obtaining [[a]] the number of circuit outputs that ~~can produce~~ produces unknown logic values at the same time includes determining the maximum number of circuit outputs that can produce errors at the same time.

Claim 11 (Canceled).

12 (Original). The compactor of claim 9 formed by a process including reducing the compactor matrix using maximum compatibility class problem.

13 (Currently Amended). The compactor of claim 12 wherein said compactor is formed of [[a]] the process including eliminating from the matrix one of at least two matching columns.

14 (Currently Amended). The compactor of claim 9 formed by [[a]] the process wherein adding at least two columns to [[a]] the compactor matrix includes adding at least two columns to the compactor matrix for every combination of the number of circuit outputs that ~~can produce~~ produces unknown logic values at the same time plus one.

15 (Currently Amended). The compactor of claim 14 formed by [[a]] the process including adding values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has the column value zero followed by the column value one and a third row has the column value zero, zero followed by the column value one.

16 (Currently Amended). A response compactor comprising:

a plurality of coupled exclusive OR gates to handle any number of scan chains with unknown logic values[[.]]; and

a control to add two columns to a compactor matrix for each scan chain that produces an unknown value at an unknown logic value at the same time as another scan chain.

17 (Previously Presented). The compactor of claim 14 to handle any number of errors in the same scan cycle.

18 (Original). The compactor of claim 14 including the minimum number of scan outputs.

19 (Currently Amended). An article comprising a medium storing instructions that, if executed, enable a ~~processor-based system~~ response compactor to:

add at least two columns to a compactor matrix for each scan chain that, at the same time as another scan chain, ~~produce~~ produces an unknown logic value.

20 (Currently Amended). The article of claim 19 further storing instructions that, if executed, enable the response compactor ~~a processor-based system~~ to obtain the maximum number of scan chains that ~~can~~ produce, at the same time, unknown logic values.

Claim 21 (Canceled).

22 (Currently Amended). The article of claim 19 further storing instructions that, if executed, enable the response compactor matrix to be reduced using maximum compatibility class problem.

23 (Currently Amended). The article of claim 19 further storing instructions that, if executed, enable the response compactor ~~a processor-based system~~ to eliminate from the matrix one of at least two matching columns.

24 (Currently Amended). The article of claim 19 further storing instructions that, if executed, enable the response compactor ~~a processor based system~~ to add at least two columns to the compactor matrix for every combination of the number of unknown logic values plus one.

25 (Currently Amended). The article of claim 23 further storing instructions that, if executed, enable the response compactor ~~a processor based system~~ to add values to the matrix rows such that for a first row the first column has a value one and the succeeding columns have the value zero and a second row has a column value zero followed by the column value one and the third row has the column value zero, zero, followed by the column value one.